IN THE SPECIFICATION:

Please replace paragraph [0030] with the following amended paragraph:

[0030] The organosilane compounds are oxidized during deposition such that the carbon content of the deposited film is between about 1% and about 50 % by atomic weight, preferably about 5% and about 50%. During deposition of the silicon oxycarbide layer, the substrate is maintained at a temperature between about -20°C and about 500°C, and preferably is maintained at a temperature between about 170°C and about 180°C.

Please replace paragraph [0044] with the following amended paragraph:

[0044] When susceptor 12 and the substrate are in processing position [[14]], they are surrounded by an insulator 17 and process gases exhaust into a manifold 24. During processing, gases inlet to manifold 11 are uniformly distributed radially across the surface of the substrate. A vacuum pump 32 having a throttle valve controls the exhaust rate of gases from the chamber.

Please replace paragraph [0074] with the following amended paragraph:

[0074] A dual damascene structure which includes two silicon oxycarbide layers and two silicon carbide cap layers or doped silicon carbide cap layers deposited thereon is shown in Fig. 5. A conductive feature 502 is disposed in substrate 500. The first silicon oxycarbide layer is deposited as a first dielectric layer 510 on a liner or barrier layer 512, for example a silicon carbide as described herein. A first silicon carbide cap layer 514 is deposited on the first dielectric layer 510 as described herein. The silicon carbide cap layer 514 reduces the dielectric constant of the silicon oxycarbide layer and is pattern etched to define the openings of vertical interconnects such as contacts/vias. For the dual damascene application, a second dielectric layer 518 comprising the second silicon

oxycarbide layer is deposited over the patterned silicon carbide cap layer 514. The second silicon carbide cap layer 519 is deposited on the second dielectric layer 518 and pattern etched to define horizontal interconnects such as lines. An etch process is performed to define the horizontal interconnects down to the first silicon carbide layer ~~314~~ 514 which functions as an etch stop, and to define the vertical interconnects and expose the conductive feature 502 in substrate 500 prior to filling the interconnects with a conductive material 526.

Please replace the abstract with the following amended abstract:

A method for processing a substrate ~~comprising~~ including depositing a dielectric layer ~~comprising~~ containing silicon, oxygen, and carbon on the substrate by chemical vapor deposition, wherein the dielectric layer has a carbon content of at least 1% by atomic weight and a dielectric constant of less than about 3, and depositing a silicon and carbon containing layer on the dielectric layer. The dielectric constant of a dielectric layer deposited by reaction of an organosilicon compound having three or more methyl groups is significantly reduced by further depositing an amorphous hydrogenated silicon carbide layer by reaction of an alkylsilane in a plasma of a relatively inert gas.